REMARKS

Claims 2 and 3 are pending. With this amendment, claims 2 and 3 are amended, and claims 1, and 4-8 have been cancelled without prejudice or disclaimer. Reconsideration of claims 2 and 3 in view of the above amendment and following remarks is respectfully requested.

The Examiner has indicated that the Information Disclosure Statement submitted February 7, 2005 is in compliance with the provisions of 37 CFR § 1.97, and has considered the citations filed therewith in part, as indicated by the Examiner's initials, and has not considered the citations filed therewith in part, as indicated by a strikethrough.

The Examiner has rejected claims 5-7 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,597,642 to Ijima et al. (Ijima). The cancellation of claims 5-7 renders the rejection of claims 5-7 under U.S.C. § 102(e) to Ijima moot.

The Examiner has rejected claims 1-4 and 8 under U.S.C. § 103(a) as being unpatentable over Ijima in view of U.S. Patent No. 4,344,165 to Akiyama (Akiyama). Applicants respectfully traverse this rejection because Ijima, either alone or in combination with Akiyama, does not disclose or suggest the combination of features recited by claims 2 and 3.

In particular, claim 2 recites a disk apparatus, including among other things:

> a combining unit which combines the first and second tracking error signals generated by the first and second variable amplifiers, and provides a combined tracking error signal;
>
> a muting unit which mutes the first tracking error signal when the first tracking error signal amplitude is lower than a predetermined reference, and mutes the second tracking error signal when the second tracking error signal amplitude is lower than a predetermined reference; and
>
> a tracking control unit which controls tracking by using the tracking error signal combined by the combining unit.

Thus, claim 2 recites *inter alia*, that a disk apparatus includes a specific combining unit which *combines* a first tracking error signal generated by a specific first variable amplifier *with* a second tracking error signal generated by a specific second variable amplifier to provide *a combined* tracking error signal and a separate muting unit which mutes the first tracking error signal, when the first tracking signal amplitude is lower than a predetermined reference and mutes the second tracking error signal when the second tracking error signal

amplitude is lower than a predetermined reference, and a tracking control unit which controls the specific tracking by using the *combined tracking error signals*.

Similarly, claim 3 recites a disk apparatus, including, among other things:

> a combining unit which combines the first and second tracking error signals generated by the first and second variable amplifiers, and provides a combined tracking error signal;
>
> a muting unit which mutes one of the first and second tracking error signals when the amplitude of the one of the tracking error signals is lower than a predetermined reference; and
>
> a tracking control unit which controls tracking by using the tracking error signal combined by the combining unit.

Thus, claim 3 recites *inter alia*, that a disk apparatus includes a combining unit which *combines* the first and second tracking error signal generated by the first and second variable amplifiers, and provides *a combined* tracking error signal and a separate muting unit which mutes one of the first and second tracking error signal when the amplitude of the one of the tracking error signals is lower than a predetermined reference, and a separate tracking control unit which controls tracking by using the *combined error signals* generated by the combining unit.

However, Ijima discloses a system that is quite different from the present invention. First, Ijima does not disclose either a structure or a process by which specifically separate and different tracking error signals are in turn combined. See, column 8, lines 29-40. In Ijima, the specific judgment 301 circuit obtains *at least three separate error signals*: the differential push-pull circuit 29 signal, the phase comparison calculation circuit 30 signal, and the three-beam calculation circuit 31 signal. Thereafter, the judgment circuit 301 selects one of the mentioned three signals and outputs that signal to the system. In Ijima, no specific signal combination is employed and clearly no separate combining unit is discussed. These deficiencies, among others, render Ijima as particularly inapplicable to claims 2-3.

Akiyama fails to make up the deficiencies noted with respect to Ijima. Akiyama does not disclose any equivalent for the separate combining unit of the present invention. Rather, Akiyama merely discloses a variable-gain amplifier 18. See, for example, Fig. 3 and column 6, lines 24-25. In Akiyama, the variable-gain amplifier 18 acts to control a separate signal received from the gain control signal generator 26. See, column 6, lines 61-69.

As Akiyama is understood, and the foregoing makes apparent, Applicants respectfully submit that Akiyma fails to disclose at least a combining unit which combines a plurality of individual tracking error signals in a manner similar to the system recited by claims 2 and 3

of the present invention. As a result, Applicants respectfully submit that Akiyama fails to describe the features as recited by claims 2-3. At least for this reason, Akiyama is not properly combinable with Ijima to render obvious claims 2-3. Therefore, Applicants respectfully submit that a *prima facie* case of obviousness has not been established with the combination of Ijima and Akiyama, and the rejection under § 103 must be withdrawn. For at least these reasons discussed above, independent claims 2 and 3 are distinguishable over the combination of Ijima and Akiyama.

In view of the above amendments and following remarks, Applicants respectfully submit that all the remaining claims are allowable and that the entire application is condition for allowance.

Should the Examiner believe that anything further is desirable to place the application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,

PILLSBURY WINTHROP SHAW PITTMAN LLP

By: _____

WILLIAM D. TITCOMB
Reg. No. 46463
Tel. No. 703.770.7847
Fax No. 703.770.7901

Date: March 15, 2007
P.O. Box 10500
McLean, VA 22102
(703) 770-7900